In the Specification:

Please amend Paragraph [0001] as follows:

[0001] This application relates to co-pending and commonly assigned patent application Serial No. 10/628,020 [[_____]], filed ~~concurrently herewith~~ July 23, 2003 and entitled "Capacitor with Improved Capacitance Density and Method of Manufacture" (TSM-03-0555), which application is hereby incorporated herein by reference.

Please amend Paragraph [0033] as follows:

[0033] According to the preferred embodiment of this invention, a heavily doped strained silicon layer or an inversion region in a strained silicon layer is used as a bottom electrode of a capacitor. The heavily doped strained silicon is preferably heavily doped with n-type dopants, and the inversion region preferably comprises electrons because the mobility of electrons is significantly increased in strained silicon. The resistance of the inversion region is inversely proportional to mobility. A high mobility inversion region has a lower resistance. Therefore, by forming a low resistance inversion layer in the strained silicon layer, and employing it as a bottom electrode of a capacitor, the capacitor is formed with an electrode with significantly improved conductance. The capacitor may be used as a decoupling capacitor in the preferred embodiment, but it is understood that the capacitor thus formed may be used for other analog or digital applications. Figure 1 shows examples of decoupling capacitors coupled between a first reference voltage line (e.g., OV_{DD}, V_{DD} or GROUND) and a second reference voltage line (e.g., OV_{DD}, V_{DD} or GROUND).